TITLE OF THE INVENTION

LIQUID CRYSTAL DEVICE, IMAGE PROCESSING DEVICE, IMAGE DISPLAY APPARATUS WITH THESE DEVICES, SIGNAL INPUT METHOD, AND IMAGE PROCESSING METHOD

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a technique of generating a common signal that is commonly supplied to respective pixels of a liquid crystal device.

2. Description of the Related Art

[0002] A liquid crystal panel is widely used as an optoelectric device for generating images. The liquid crystal panel is an optoelectric device that applies a voltage corresponding to a display signal to liquid crystal forming respective pixels and regulates the light transmittance of each pixel, so as to generate an image in response to the display signal.

[0003] In the prior art liquid crystal panel, a common signal representing a standard level of the display signal is input via an exclusively provided input terminal, separately from the display signal. An electronic apparatus, such as an image display apparatus, with the prior art liquid crystal panel, accordingly has a common signal generation circuit for generating the common signal.

[0004] Different offset values depending on respective devices are set to the level of the common signal. The common signal generation circuit is thus constructed to enable adjustment of the level of the common signal

according to the generated offset.

[0005] In order to enhance the reliability of the liquid crystal panel and reduce the manufacturing cost, however, it is desirable to reduce the total number of input terminals for receiving externally supplied signals.

[0006] In order to enhance the reliability of the electronic apparatus with the liquid crystal panel, reduce the size of the electronic apparatus, simplify the structure of the electronic apparatus, and reduce the manufacturing cost, it is also desirable to omit the common signal generation circuit.

SUMMARY OF THE INVENTION

[0007] The object of the present invention is thus to provide a technique that enhances the reliability of a liquid crystal panel, as well as enhances the reliability of an electronic apparatus with the liquid crystal panel, reduces the size of the electronic apparatus, simplifies the structure of the electronic apparatus, and reduces the manufacturing cost.

[0008] At least part of the above and the other related objects is attained by a liquid crystal device having multiple pixels. The liquid crystal device includes an input terminal that receives a display signal including multiple pixel signals to be supplied to the multiple pixels, the display signal having a predetermined signal embedded therein for generating a common signal, which is to be commonly supplied to the multiple pixels, during a predetermined period that does not include the pixel signals in the display signal.

[0009] The liquid crystal device of the present invention inputs the display signal with the predetermined signal embedded therein. The

predetermined signal, which is used for generating the common signal to be commonly supplied to the multiple pixels, is embedded in the display signal that includes the multiple pixel signals to be given to the multiple pixels. This arrangement allows omission of the input terminal exclusively provided for inputting the common signal in the prior art liquid crystal device, thus desirably enhancing the reliability of the liquid crystal device.

[0010] It is desirable that the predetermined period is part of a horizontal scanning period except an effective horizontal scan period. It is also desirable that the predetermined period is part of a vertical scanning period except an effective vertical scan period.

[0011] Either of the above periods does not include the multiple pixel signals in the display signal, so that the predetermined signal for generating the common signal can readily be embedded in the display signal.

[0012] In accordance with one preferable application of the present invention, the liquid crystal device further includes: a common signal line that is commonly connected to the multiple pixels; and a common signal line driving circuit that generates the common signal in response to the predetermined signal included in the display signal input from the input terminal and supplies the generated common signal to the common signal line.

[0013] In this application, the common signal line driving circuit functions to readily supply the common signal to the multiple pixels via the common signal line.

[0014] The common signal line driving circuit may be a sample/hold circuit that samples the predetermined signal included in the display signal

input from the input terminal and outputs the predetermined sampled signal as the common signal.

[0015] In accordance with one preferable embodiment, the liquid crystal device further has: multiple rows of scanning lines and multiple columns of signal lines for selecting the multiple pixels; a scanning line driving circuit that supplies scanning signals to the corresponding multiple rows of scanning lines in a sequence of the multiple rows of scanning lines; and a signal line driving circuit that samples display signals corresponding to the multiple columns of signal lines in a sequence of the multiple columns of signal lines and supplies the sampled display signals to the corresponding signal lines. The signal line driving circuit supplies a sample/hold signal, which is used for sampling the predetermined signal, to the common signal line driving circuit.

[0016] This arrangement enables the sample/hold signal, which is used for sampling the predetermined signal, to be readily supplied to the common signal line driving circuit during part of a horizontal scanning period except an effective horizontal scan period.

[0017] In accordance with another preferable embodiment, the liquid crystal device further has: multiple rows of scanning lines and multiple columns of signal lines for selecting the multiple pixels; a scanning line driving circuit that supplies scanning signals to the corresponding multiple rows of scanning lines in a sequence of the multiple rows of scanning lines; and a signal line driving circuit that samples display signals corresponding to the multiple columns of signal lines in a sequence of the multiple columns of signal lines and supplies the sampled display signals to the corresponding signal lines. The scanning line driving circuit supplies a sample/hold

signal, which is used for sampling the predetermined signal, to the common signal line driving circuit.

[0018] This arrangement enables the sample/hold signal, which is used for sampling the predetermined signal, to be readily supplied to the common signal line driving circuit during part of a vertical scanning period except an effective vertical scan period.

[0019] The present invention is also directed to an image processing device that generates a display signal, which is to be input into a liquid crystal device having multiple pixels. The image processing device includes: a video signal conversion circuit that converts an input video signal and generates multiple pixel signals, which are to be given to the multiple pixels of the liquid crystal device; and a display signal generation circuit that combines the multiple pixel signals with a predetermined signal, which is used for generating a common signal to be commonly supplied to the multiple pixels, and thereby generates one display signal.

[0020] The image processing device of the present invention readily generates the display signal, which is to be input into the liquid crystal device of the present invention.

[0021] The present invention is further directed to an image display apparatus, which includes: a liquid crystal device having multiple pixels; and an image processing device that generates a display signal, which is to be input into the liquid crystal device. The liquid crystal device has an input terminal that receives the display signal including multiple pixel signals to be supplied to the multiple pixels, the display signal having a predetermined signal embedded therein for generating a common signal, which is to be commonly supplied to the multiple pixels, during a

predetermined period that does not include the pixel signals in the display signal. The image processing device includes: a video signal conversion circuit that converts an input video signal and generates the multiple pixel signals, which are to be given to the multiple pixels of the liquid crystal device; and a display signal generation circuit that combines the multiple pixel signals with a predetermined signal, which is used for generating a common signal to be commonly supplied to the multiple pixels, and thereby generates one display signal.

[0022] The image display apparatus of the present invention includes the liquid crystal device and the image processing device of the present invention. The enhanced reliability of the liquid crystal device leads to enhancement of the reliability of the image display apparatus. This arrangement also enables omission of the common signal generation circuit, which is required in the prior art image display apparatus. This enhances the reliability of the image display apparatus, reduces the size of the image display apparatus, simplifies the structure of the image display apparatus, and reduces the manufacturing cost.

[0023] In accordance with one preferable application of the image display apparatus, the image processing device further includes an adjustment control circuit that adjusts a value of data included in the predetermined signal.

[0024] This arrangement enables the value of the common signal, which varies depending upon the liquid crystal device, to be readily adjusted.

[0025] The technique of the present invention may be actualized in a diversity of applications other than the liquid crystal device, the image processing device, and the image display apparatus discussed above; for

example, a method of inputting the predetermined signal, which is used for generating the common signal to be commonly supplied to multiple pixels of the liquid crystal device, and an image processing method to generate the display signal that is to be input into the liquid crystal device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] Fig. 1 is a circuit diagram schematically illustrating the electric structure of a liquid crystal panel 10 in a first embodiment of the present invention;

Fig. 2 is a timing chart showing operations of a scanning line driving circuit 500 included in the liquid crystal panel 10;

Fig. 3 is a timing chart showing operations of a signal line driving circuit 200 and a common signal line driving circuit 400 included in the liquid crystal panel 10;

Fig. 4 is a circuit diagram schematically illustrating the electric structure of a liquid crystal panel 10A in a second embodiment of the present invention;

Fig. 5 is a timing chart showing operations of a scanning line driving circuit 500A included in the liquid crystal panel 10A;

Fig. 6 is a block diagram schematically illustrating the construction of an image display apparatus DP1 with the liquid crystal panel 10 of the present invention applied thereto;

Fig. 7 is a timing chart showing a process of generating a display signal VIN supplied to the liquid crystal panel 10;

Fig. 8 is a block diagram schematically illustrating the construction of another image display apparatus DP2 with the liquid crystal panel 10 of

the present invention applied thereto; and

Fig. 9 is a timing chart showing a process of generating the display signal VIN supplied to the liquid crystal panel 10.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0027] Some modes of carrying out the present invention are discussed below as preferred embodiments in the following sequence:

A. Construction and Operations of Liquid Crystal Panel

A1. First Embodiment of Liquid Crystal Panel

A2. Second Embodiment of Liquid Crystal Panel

B. Construction and Operations of Image Display Apparatus with Liquid Crystal Panel

B1. First Embodiment of Image Display Apparatus

B2. Second Embodiment of Image Display Apparatus

C. Modifications

[0028] A. Structure and Operations of Liquid Crystal Panel

A1. First Embodiment of Liquid Crystal Panel

Fig. 1 is a circuit diagram schematically illustrating the electric structure of a liquid crystal panel 10 in a first embodiment of the present invention. The liquid crystal panel 10 includes an image display module 100, a signal line driving circuit 200, a sampling circuit 300, a common signal line driving circuit 400, and a scanning line driving circuit 500. The liquid crystal panel 10 has input terminals to receive an analog display signal VIN as well as a vertical synchronizing signal VRST, a horizontal synchronizing signal HRST, a vertical clock signal VCLK, and a horizontal

clock signal HCLK as timing signals. Circuits that are not essential elements of the present invention, such as a pre-charge circuit, and input terminals, such as a power input terminal, are omitted from the illustration of the liquid crystal panel 10. In the description below, identical symbols are allocated to input terminals, signal lines, and signals.

[0029] The image display module 100 has matrix wiring consisting of 'n' (where 'n' is an integer of not less than 2) scanning lines SL (SL1 to SLn) running in a horizontal direction and 'm' (where 'm' is an integer of not less than 2) signal lines DL (DL1 to DLm) running in a vertical direction. Pixels PE are provided on respective intersections in the matrix wiring.

[0030] Each pixel PE of the image display module 100 includes a TFT (Thin Film Transistor) 110 for pixel selection and a liquid crystal pixel 120 having a liquid crystal cell (not shown). A gate electrode (G) of the TFT 110 is connected to the corresponding scanning line SL and a drain electrode (D) is connected to the corresponding signal line DL, while a source electrode (S) is connected to a pixel electrode 121 of the liquid crystal pixel 120. The liquid crystal pixel 120 includes the pixel electrode 121, a common electrode 122, and liquid crystal interposed between the pixel electrode 121 and the common electrode 122. The common electrode 122 is connected to a common signal line VCOM. All the pixels PE arrayed in 'n' lines by 'm' columns are accordingly connected to the common signal line VCOM via the common electrodes 122 of the liquid crystal pixels 120.

[0031] The 'n' rows of scanning lines SL are connected to the scanning line driving circuit 500. The 'm' columns of signal lines DL are connected to a display signal line VIN via the sampling circuit 300. The common signal line VCOM is connected to the display signal line VIN via the

common signal line driving circuit 400.

[0032] The sampling circuit 300 is provided with switches SW (SW1 to SWm) corresponding to the respective data lines DL. Each switch SW is constructed by a semiconductor element, such as a TFT. A drain electrode (D) of each switch SW is commonly connected to the display signal line VIN and each source electrode (S) is connected to the corresponding signal line DL, while each gate electrode (G) is connected to the signal line driving circuit 200 via a corresponding sampling signal line GS (GS1 to GSm). The sampling circuit 300 functions to sample the display signal VIN and supply the sampled display signal VIN to each signal line DL, in response to each sampling signal GS transmitted from the signal line driving circuit 200.

[0033] The common signal line driving circuit 400 is a sample/hold circuit including a switch 410, a capacitor 420, and a buffer amplifier 430. Like the switch SW of the sampling circuit 300, the switch 410 is constructed by a semiconductor element. A drain electrode (D) of the switch 410 is connected to the display signal line VIN, and a source electrode (S) is connected to one terminal of the capacitor 420 and an input terminal of the buffer amplifier 430. A gate electrode (G) of the switch 410 is connected to the signal line driving circuit 200 via a sample/hold driving signal line SH. The other terminal of the capacitor 420 is grounded. The common signal line driving circuit 400 samples and holds the display signal VIN in response to a sample/hold driving signal SH and generates a common signal VCOM as discussed later.

[0034] The scanning line driving circuit 500 applies scanning line signals (pulse signals) to the respective scanning lines SL in a line sequential manner at preset timings, in response to the vertical

synchronizing signal VRST and the vertical clock signal VCLK, as discussed later.

[0035] The signal line driving circuit 200 applies sampling signals (pulse signals) to the respective sampling signal lines GS in a line sequential manner at the timings of application of the scanning signals to the respective scanning lines SL by the scanning line driving circuit 500, in response to the horizontal synchronizing signal HRST and the horizontal clock signal HCLK, as discussed later. The signal line driving circuit 200 also applies sample/hold driving signals (pulse signals) to the sample/hold driving signal line SH. The sampling circuit 300 and the signal line driving circuit 200 correspond to the signal line driving circuit of the present invention.

[0036] Fig. 2 is a timing chart showing operations of the scanning line driving circuit 500 included in the liquid crystal panel 10. The vertical synchronizing signal VRST, the vertical clock signal VCLK, the horizontal synchronizing signal HRST, and the horizontal clock signal HCLK as the timing signals are input at timings shown in Figs. 2(a) through 2(d). The vertical synchronizing signal VRST shown in Fig. 2(a) is a periodic signal representing a start timing of vertical scanning. One period of the pulse signal starting from a falling edge represents a vertical scanning period (vertical scanning cycle) V for displaying one frame image.

[0037] The vertical clock signal VCLK shown in Fig. 2(b) is synchronous with the vertical synchronizing signal VRST and represents an activation timing of the scanning line driving circuit 500, that is, a driving period of each scanning line SL. In the specification hereof, the expression of 'synchronize' means that two signals vary with a fixed phase.

[0038] In the vertical clock signal VCLK, one period of the pulse signal starting from a rising edge represents a driving period of one scanning line SL, that is, a horizontal scanning period (horizontal scanning cycle) H. The vertical scanning period V is set to be equal to (8+n)-fold horizontal scanning period H, that is, a period (8+n)H. In the following description, the first horizontal scanning period, the second horizontal scanning period, ... and the (8+n)-th horizontal scanning period are respectively referred to as '1H period', '2H period', ... and '(8+n)H period'.

[0039] The horizontal synchronizing signal HRST shown in Fig. 2(c) is a pulse signal rising at substantially the same timing as that of the vertical clock signal VCLK of Fig. 2(b). The horizontal synchronizing signal HRST is a periodic signal representing a start timing of horizontal scanning discussed later. The horizontal synchronizing signal HRST is generally set to have a narrower pulse width at high level, compared with the vertical clock signal VCLK.

[0040] The horizontal clock signal HCLK shown in Fig. 2(d) is synchronous with the horizontal synchronizing signal HRST and represents an activation timing of the signal line driving circuit 200, that is, a drive timing of each signal line DL, as described later. Either one of the vertical clock signal VCLK and the horizontal synchronizing signal HRST may be omitted.

[0041] Signals to be given to pixels actuated by the respective scanning lines SL are supplied as the display signal VIN in a time period EV from the 6H period to the (5+n)H period (hereinafter referred to as the 'effective vertical scan period') in each vertical scanning period V as shown in Fig. 2(e). The signal given as the display signal VIN is supplied synchronously with

the horizontal synchronizing signal HRST and the horizontal clock signal HCLK discussed later.

[0042] The scanning line driving circuit 500 supplies high-level pulse signals as scanning line signals to the corresponding scanning lines SL (SL1 to SLn) in a line sequential manner in the respective horizontal scan periods 6H to (5+n)H of the effective vertical scan period EV as shown in Figs. 2(f-1) through 2(f-n). The scanning line driving circuit 500 is readily constructed by a shift register, which utilizes the vertical clock signal VCLK as a shift clock.

[0043] Fig. 3 is a timing chart showing operations of the signal line driving circuit 200 and the common signal line driving circuit 400 included in the liquid crystal panel 10. This timing chart shows the 6H period, that is, the 6th horizontal scanning period of Fig. 2. Figs. 3(a) and 3(b) show the horizontal synchronizing signal HRST and the horizontal clock signal HCLK of Figs. 2(c) and 2(d), respectively. Fig. 3(c) shows the display signal VIN of Fig. 2(e).

[0044] In the horizontal clock signal HCLK shown in Fig. 3(c), one period of the pulse signal starting from a falling edge represents a driving period of one signal line DL, that is, a pixel period T. The horizontal scanning period H is set to be equal to (4+m)-fold pixel period T, that is, a period (4+m)T. In the following description, the first pixel period, the second pixel period, ... and the (4+m)-th pixel period are respectively referred to as '1T period', '2T period', ... and '(4+m)T period'.

[0045] Signals P1 to Pm to be given to the respective signal lines DL (DL1 through DLm) are supplied as the display signal VIN synchronously with the horizontal clock signal HCLK in a time period EH from the 4T

period to the (3+m)T period (hereinafter referred to as the 'effective horizontal scan period') as shown in Fig. 3(c).

A signal COM corresponding to the common signal VCOM is supplied as the display signal VIN synchronously with the horizontal clock signal HCLK in a time period from the 2T period to the 3T period (hereinafter referred to as the 'common signal generation period').

[0046] The signal line driving circuit 200 supplies a high-level pulse signal to the sample/hold driving signal line SH in the common signal generation period as shown in Fig. 3(d). The common signal line driving circuit 400 samples the level of the signal COM supplied as the display signal VIN and outputs the sampled signal level as the common signal VCOM as shown in Fig. 3(f). The common signal line driving circuit 400 functions to keep the common signal VCOM at the signal level specified by the sampled signal COM while the sample/hold driving signal SH is kept at the low level, that is, before the sample/hold driving signal SH rises to the high level.

[0047] As shown in Figs. 3(e-1) through 3(e-m), the signal line driving circuit 200 supplies high-level pulse signals as sampling signals to the corresponding sampling signal lines GS (GS1 to GSm) in a line sequential manner in the respective pixel periods 4T to (3+m)T of the effective horizontal scan period EH. The signals P1 to Pm given to the display signal line VIN are supplied to the corresponding signal lines DL1 to DLm in a line sequential manner in each pixel period of the effective horizontal scan period EH. The signal line driving circuit 200 may readily be constructed by a shift register that utilizes the horizontal clock signal HCLK as a shift clock.

[0048] The above procedure activates the pixels PE connecting with the scanning lines SL and the signal lines DL selected by the scanning line driving circuit 500 and the signal line driving circuit 200. The display signal VIN supplied to the pixel PE in the active state via the sampling circuit 300 is applied to the pixel electrode 121 of the liquid crystal pixel 120. The common signal VCOM supplied via the common signal line driving circuit 400 is, on the other hand, applied to the common electrode 122 of the liquid crystal pixel 120. The liquid crystal pixel 120 works according to a potential difference between these two electrodes 121 and 122. Such activation enables an image to be displayed according to the supplied display signal in the image display module 100.

[0049] As described above, in this liquid crystal panel 10, the common signal line driving circuit 400 samples and holds the signal COM, which corresponds to the common signal VCOM and is supplied via the display signal input terminal VIN in the pixel periods 2T and 3T (the common signal generation period) immediately before the start of the effective horizontal scan period EH. This results in generating the common signal VCOM, which is to be supplied to each pixel PE. This liquid crystal panel 10 does not require a specifically provided input terminal, which is used in the prior art liquid crystal panel, to supply the common signal VCOM. This desirably reduces the total number of input terminals and thereby enhances the reliability of the device.

[0050] In the liquid crystal panel 10 of this embodiment, the two pixel periods 2T and 3T immediately before the effective horizontal scan period EH are set as the common signal generation period. Only one pixel period or a time period of three or greater pixel periods may alternatively be set as

the common signal generation period. A time period immediately after the effective horizontal scan period EH may be set as the common signal generation period. Namely the common signal generation period may be set in an adequate time period except the effective horizontal scan period EH. The signal line driving circuit 200 of the liquid crystal panel 10 is constructed to output the sample/hold driving signal SH corresponding to the preset common signal generation period.

[0051] A2. Second Embodiment of Liquid Crystal Panel

Fig. 4 is a circuit diagram schematically illustrating the electric structure of a liquid crystal panel 10A in a second embodiment of the present invention. The liquid crystal panel 10A is characterized by that a gate electrode (G) of a switch 410 included in a common signal line driving circuit 400A is connected to a scanning line driving circuit 500A via a sample/hold driving signal line SV, whereas the common signal line driving circuit 400 (Fig.1) in the liquid crystal panel 10 of the first embodiment is connected to the signal line driving circuit 200 via the sample/hold driving signal line SH.

[0052] Fig. 5 is a timing chart showing operations of the scanning line driving circuit 500A included in the liquid crystal panel 10A. Figs. 5(a) through 5(d) and Figs. 5(f-1) through 5(f-n) are identical with Figs. 2(a) through 2(d) and Figs. 2(f-1) through 2(f-n).

[0053] The scanning line driving circuit 500A supplies a high-level pulse signal to the sample/hold driving signal line SV shown in Fig. 5(g) in a horizontal scanning period 5H (common signal generation period) immediately before the start of the effective vertical scan period EV. The

common signal line driving circuit 400A samples the level of the signal COM corresponding to the common signal VCOM supplied as the display signal VIN and holds the sampled signal level during the low signal level, thus generating the common signal VCOM.

[0054] In this manner, the liquid crystal panel 10A of this embodiment samples the level of the signal COM corresponding to the common signal VCOM supplied as the display signal VIN in the common signal generation period set immediately before the effective vertical scan period and thereby generates the common signal VCOM.

[0055] The liquid crystal panel 10A of this construction does not require a specifically provided input terminal, which is used in the prior art liquid crystal panel, to supply the common signal VCOM. This desirably reduces the total number of input terminals and thereby enhances the reliability of the device.

[0056] In the liquid crystal panel 10A of this embodiment, one horizontal scanning period 5H immediately before the effective vertical scan period EV is set as the common signal generation period. A time period of two or greater horizontal scanning periods may alternatively be set as the common signal generation period. A time period immediately after the effective vertical scan period EV may be set as the common signal generation period. Namely the common signal generation period may be set in an adequate time period except the effective vertical scan period EV. The scanning line driving circuit 500A of the liquid crystal panel 10A is constructed to output the sample/hold driving signal SV corresponding to the preset common signal generation period.

[0057] B. Construction and Operations of Image Display Apparatus with Liquid Crystal Panel

B1. First Embodiment of Image Display Apparatus

Fig. 6 is a block diagram schematically illustrating the construction of an image display apparatus DP1 with the liquid crystal panel 10 of the present invention applied thereto. The image display apparatus DP1 includes the liquid crystal panel 10, an image processing circuit 20, and a D-A converter 30. The image processing circuit 20 has a video signal conversion circuit 22, a COM signal generation circuit 24, and a timing control circuit 26. The timing control circuit 26 generates the timing signals supplied to the liquid crystal panel 10, that is, the vertical synchronizing signal VRST, the horizontal synchronizing signal HRST, the vertical clock signal VCLK, and the horizontal clock signal HCLK, as well as a polarity inversion signal VINV that controls the output polarity of the D-A converter 30 as discussed later. The timing control circuit 26 controls the operations of the video signal conversion circuit 22 and the COM signal generation circuit 24.

[0058] The video signal conversion circuit 22 converts a video signal supplied from an image supply apparatus (not shown), such as a personal computer or a video recorder, into a video signal of a specific timing that enables supply to the liquid crystal panel 10, and outputs the converted video signal. More concretely, the video signal conversion circuit 22 converts an analog video signal into digital video data and writes the converted digital video data into a frame memory (not shown) included in the video signal conversion circuit 22 synchronously with a synchronizing signal. The video signal conversion circuit 22 also reads the digital video

data, which has been written in its frame memory, at specific timings that enable supply to the liquid crystal panel 10, that is, based on the timing signals VRST, HRST, VCLK, and HCLK generated by the timing control circuit 26. Diverse series of image processing are carried out in the writing and reading processes. In the case where the video signal supplied from the image supply apparatus is not an analog video signal but a digital video signal, the conversion of the analog video signal into the digital video data is omitted.

[0059] The COM signal generation circuit 24 combines the signal COM corresponding to the signal level to be supplied to the common signal line VCOM with the digital video signal VDT output from the video signal conversion circuit 22 to a composite signal and outputs the composite signal as a digital display signal VDATA.

[0060] The D-A converter 30 converts the digital display signal VDATA output from the image processing circuit 20 into an analog video signal and supplies the converted analog video signal as the display signal VIN to the liquid crystal panel 10. The polarity inversion signal VINV is supplied from the timing control circuit 26 to the D-A converter 30. As discussed later, the polarity of the output signal from the D-A converter 30 is inverted in response to the polarity inversion signal VINV output from the timing control circuit 26 synchronously with the vertical synchronizing signal VRST and the horizontal synchronizing signal HRST.

[0061] Fig. 7 is a timing chart showing a process of generating the display signal VIN supplied to the liquid crystal panel 10. This timing chart shows the first horizontal scanning period 6H in the effective vertical scan period EV shown in Fig. 2. The relation between the horizontal

synchronizing signal HRST and the horizontal clock signal HCLK shown in Figs. 7(a) and 7(b) is identical with the relation between Figs. 3(a) and 3(b). The relations between the vertical synchronizing signal VRST, the vertical clock signal VCLK, the horizontal synchronizing signal HRST, the horizontal clock signal HCLK, and the display signal VIN in this embodiment are identical with those of Fig. 2 and are thus not specifically illustrated or explained here. The other horizontal scanning periods included in the effective vertical scan period EV are identical with those of Fig. 2, except the timing of the polarity inversion signal VINV discussed later, and are thus not specifically described here.

[0062] The video signal conversion circuit 22 outputs pixel data P1 to Pm corresponding to respective pixel periods as the digital video signal VDT in the effective horizontal scan period EH (pixel periods 4T to (3+m)T) as shown in Fig. 7(c). The digital video signal VDT corresponds to the timing conversion signal of the present invention. The COM signal generation circuit 24 combines the signal COM representing the common signal VCOM with the digital video signal VDT to a composite signal in the pixel periods 2T and 3T (the common signal generation period) immediately before the effective horizontal scan period EH and outputs the composite signal as the digital display signal VDATA as shown in Fig. 7(d).

[0063] The timing control circuit 26 supplies the polarity inversion signal VINV, which repeats a high (negative) level and a low (positive) level in each horizontal scanning period as shown in Fig. 7(e), to the D-A converter 30. The polarity inversion signal VINV is controlled to keep the high (negative) level in the common signal generation period, because of the reason discussed below. In the horizontal scanning period 6H shown in Fig.

7(e), the polarity inversion signal VINV is expected to change its signal level from the high (negative) level to the low (positive) level at a rising timing of the horizontal synchronizing signal HRST. The polarity inversion signal VINV is, however, not changed to the low (positive) level but is kept at the high (negative) level during the pixel periods 1T to 3T.

[0064] The D-A converter 30 converts the digital display signal VDATA into an analog signal and outputs the converted analog signal as the analog display signal VIN as shown in Fig. 7(f). The D-A converter 30 inverts the polarity of its output according to the level of the polarity inversion signal VINV. The inversion follows the series of processing discussed below.

[0065] The video signal supplied to the video signal conversion circuit 22 represents 8-bit tone data; '0' represents the black level and '255' represents the white level. In the image display apparatus DP1 of this embodiment, the video signal conversion circuit 22 and the COM signal generation circuit 24 output the digital video signal VDT and the digital display signal VDATA as 8-bit tone data, which includes '0' representing the black level and '255' representing the white level. At the low (positive) level of the polarity inversion signal VINV, the D-A converter 30 outputs a center voltage Vc to the tone data '0' of the black level, while outputting a higher level voltage (Vc+Vf) than the center voltage Vc by a voltage Vf to the tone data '255' of the white level. At the high (negative) level of the polarity inversion signal VINV, on the other hand, the D-A converter 30 outputs he center voltage Vc to the tone data '0' of the black level, while outputting a lower level voltage (Vc−Vf) than the center voltage Vc by the voltage Vf to the tone data '255' of the white level. Namely the D-A converter 30 converts data of the digital display signal VDATA into the analog video signal VIN with the inverted

polarity about the center voltage Vc, in response to the polarity inversion signal VINV.

[0066] Application of a DC voltage to liquid crystal forming the pixels for a long time deteriorates the liquid crystal. Inversion of the polarity of the display signal VIN suppresses the deterioration and extends the life of the liquid crystal panel. The inversion of the polarity is not restricted in the horizontal scanning period, but it is preferable to invert the polarity of the signal applied to the respective pixels in each frame period or vertical scanning period.

[0067] The polarity inversion signal VINV is not changed to the low (positive) level but is kept at the high (negative) level during the pixel periods 1T to 3T in the horizontal scanning period, in which the polarity inversion signal VINV is expected to change from the high (negative) level to the low (positive) level at a rising timing of the horizontal synchronizing signal HRST, because of the following reason. The level of the common signal VCOM is ideally set to be equal to the center voltage Vc of the display signal VIN. The actual level of the common signal VCOM is, however, generally lower than the center voltage Vc. The output of the D-A converter 30 is higher than the center voltage Vc at the low (positive) level of the polarity inversion signal VINV. In the case where the polarity inversion signal VINV is at the low (positive) level during the common signal generation period, the D-A converter 30 can not output the voltage corresponding to the actual level of the common signal VCOM. This is why the polarity inversion signal VINV is not changed to the low (positive) level but is kept at the high (negative) level during the pixel periods 1T to 3T in the horizontal scanning period, in which the polarity inversion signal VINV

is expected to change from the high (negative) level to the low (positive) level at a rising timing of the horizontal synchronizing signal HRST, that is, the polarity inversion signal VINV is kept at the high (negative) level during the common signal generation period. In the image display apparatus DP1 of this embodiment, the level of the common signal VCOM is set equal to the tone data '55'.

[0068] In the image display apparatus DP1 of this embodiment, the timing control circuit 26 of the image processing circuit 20 generates the timing signals VRST, HRST, VCLK, and HCLK, which are to be supplied to the liquid crystal panel 10. The COM signal generation circuit 24 of the image processing circuit 20 outputs the signal COM, which represents the common signal VCOM during the common signal generation period, as the digital display signal VDATA. The D-A converter 30 then converts the digital display signal VDATA into the analog display signal VIN. Such arrangement completes the image display apparatus with the liquid crystal panel 10 applied thereto.

[0069] As clearly understood from the above description, the COM signal generation circuit 24 and the D-A converter 30 correspond to the display signal generation circuit of the present invention. The image processing circuit 20 and the D-A converter 30 correspond to the image processing device of the present invention.

[0070] In one possible application, the image display apparatus DP1 may be provided with a controller that controls the whole apparatus. The user may change (adjust) the value of the tone data specified by the signal COM generated by the COM signal generation circuit 24 of the image processing circuit 20 via the controller. This enables the level of the

common signal VCOM to be readily adjusted in the liquid crystal panel 10. In this application, the controller corresponds to the adjustment control circuit of the present invention.

[0071] B2. Second Embodiment of Image Display Apparatus

Fig. 8 is a block diagram schematically illustrating the construction of another image display apparatus DP2 with the liquid crystal panel 10 of the present invention applied thereto. The image display apparatus DP2 includes the liquid crystal panel 10, an image processing circuit 20A, and a D-A converter 30A. The image processing circuit 20A has a video signal conversion circuit 22A, a COM signal generation circuit 24A, and a timing control circuit 26A. The functions of the respective circuits 22A through 26A of the image processing circuit 20A and the D-A converter 30A are basically identical with those of the respective circuits 22 through 26 of the image processing circuit 20 and the D-A converter 30 (see Fig. 6). The following description focuses on the difference between the image display apparatus DP2 and the image display apparatus DP1.

[0072] Fig. 9 is a timing chart showing a process of generating the display signal VIN supplied to the liquid crystal panel 10. Like the timing chart of Fig.7, this timing chart shows the first horizontal scanning period 6H in the effective vertical scan period EV shown in Fig. 2. The relation between the horizontal synchronizing signal HRST and the horizontal clock signal HCLK shown in Figs. 9(a) and 9(b) is identical with the relation between Figs. 3(a) and 3(b). The relations between the vertical synchronizing signal VRST, the vertical clock signal VCLK, the horizontal synchronizing signal HRST, the horizontal clock signal HCLK, and the

display signal VIN in this embodiment are identical with those of Fig. 2 and are thus not specifically illustrated or explained here.

[0073] The timings of the digital video signal VDT shown in Fig. 9(c) and the digital display signal VDATA shown in Fig. 9(d) are identical with those of Figs. 7(c) and 7(d).

[0074] The values of the tone data output from the video signal conversion circuit 22A and the COM signal generation circuit 24A of the image processing circuit 20A in the image display apparatus DP2 of this embodiment are different from the tone data output from the video signal conversion circuit 22 and the COM signal generation circuit 24 of the image processing circuit 20 in the image display apparatus DP1 of the first embodiment, as discussed below.

[0075] The video signal supplied to the video signal conversion circuit 22A is 8-bit tone data, which includes '0' representing the black level and '255' representing the white level. In the image display apparatus DP2 of this embodiment, the video signal conversion circuit 22A outputs the digital video signal VDT and the digital display signal VDATA as 9-bit tone data. More specifically, the video signal conversion circuit 22A sets '255' to the tone data of the black level and '511' to the tone data of the white level, in the case of no inversion of the polarity of the display signal. In the case of inversion of the polarity of the display signal, on the other hand, the video signal conversion circuit 22A sets '255' to the tone data of the black level and '0' to the tone data of the white level. The COM signal generation circuit 24A correspondingly outputs the tone data representing the common signal VCOM as 9-bit data. In this embodiment, the level of the common signal VCOM is set equal to the tone data of '200'.

[0076] The D-A converter 30A converts the 9-bit digital video signal VDATA output from the image processing circuit 20A into the analog display signal VIN. The tone data '255' corresponding to the black level is accordingly converted to the center voltage Vc, while the tone data '511' corresponding to the white level of the positive polarity and the tone data '0' corresponding to the white level of the negative polarity are respectively converted to a voltage (Vc+Vf) and a voltage (Vc−Vf). The image processing circuit 20A and the D-A converter 30A thus generate the display signal VIN, which is to be supplied to the liquid crystal panel 10, in the same manner as that of the image processing circuit 20 and the D-A converter 30.

[0077] In the image display apparatus DP2 of this embodiment, the timing control circuit 26A of the image processing circuit 20A generates the timing signals VRST, HRST, VCLK, and HCLK, which are to be supplied to the liquid crystal panel 10. The COM signal generation circuit 24A of the image processing circuit 20A outputs the signal COM, which represents the common signal VCOM during the common signal generation period, as the digital display signal VDATA. The D-A converter 30A then converts the digital display signal VDATA into the analog display signal VIN. Such arrangement completes the image display apparatus with the liquid crystal panel 10 applied thereto.

[0078] As clearly understood from the above description, the COM signal generation circuit 24A and the D-A converter 30A correspond to the display signal generation circuit of the present invention. The image processing circuit 20A and the D-A converter 30A correspond to the image processing device of the present invention.

[0079] Like the image display apparatus DP1 of the first embodiment, in

one possible application, this image display apparatus DP2 may be provided with a controller that controls the whole apparatus. The user may change (adjust) the value of the tone data specified by the signal COM generated by the COM signal generation circuit 24A of the image processing circuit 20A via the controller. This enables the level of the common signal VCOM to be readily adjusted in the liquid crystal panel 10.

[0080] C. Modifications

The present invention is not restricted to the above embodiments or their applications, but there may be many other modifications, changes, and alterations without departing from the scope or spirit of the main characteristics of the present invention. Some examples of possible modification are given below.

[0081] The image display apparatuses DP1 and DP2 of the above embodiments include the liquid crystal panel 10 of the first embodiment, although they may include the liquid crystal panel 10A of the second embodiment instead. In the image display apparatus with the liquid crystal panel 10A, the COM signal generation circuit of the image processing circuit generates the signal COM representing the common signal VCOM during the common signal generation period corresponding to the liquid crystal panel 10A.

[0082] The above embodiments regard the image display apparatuses that display images supplied from an external image supply apparatus, as the electronic apparatus with the liquid crystal panel 10 of the present invention applied thereto. The technique of the present invention is, however, not restricted to these embodiments, but may be applicable to

diverse electronic equipment including an image processing apparatus, a D-A converter, and a liquid crystal panel.